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A METHOD AND DEVICE FOR ECHO CANCELLATION IN A TRANSMISSION DEVICE, SUCH AS A MODEM

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(54) A method and device for echo cancellation in a transmission device, such as a modem

(57) In a method for echo cancellation in a transmission device, such as a modem, an echo estimate ($B_mB_{m-1}...B_{m-N+1}...B_0$) is formed of the transmitted signal and said echo estimate is subtracted from the received signal. To reduce the requirements on the necessary A/D and D/A converters, N most significant bits ($B_mB_{m-1}...B_{m-N+1}$) are separated from the echo estimate and the portion of the echo estimate corresponding to these is analogically (14) subtracted from the received signal, and the portion of the echo estimate corresponding to the remaining least significant bits ($B_{m-N}...B_0$) thereof is digitally (12) eliminated from the received signal.

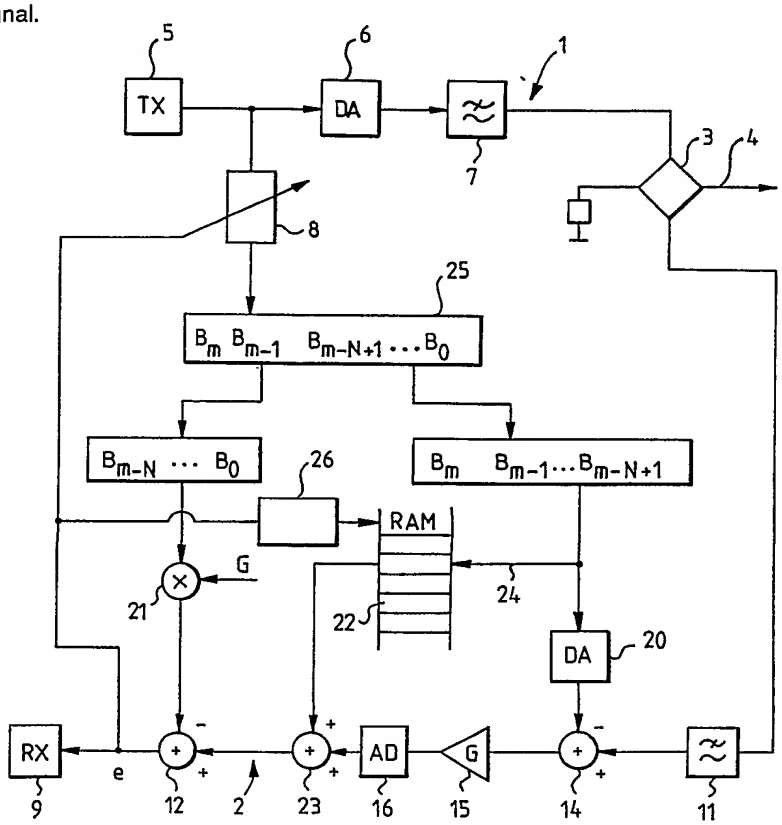

FIG. 3

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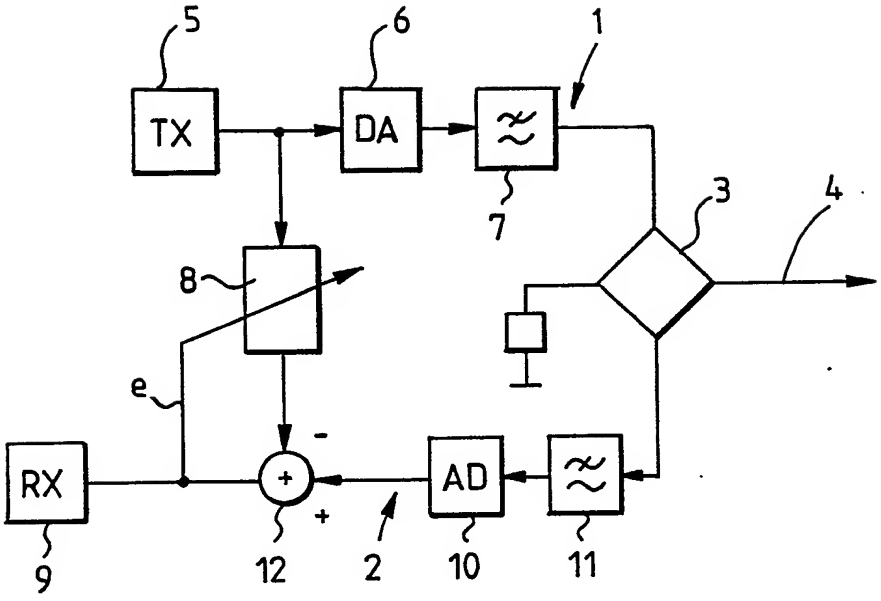
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6
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TX
DA
7
3
4
8
e
RX
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9
12
2
10
11

FIG. 1

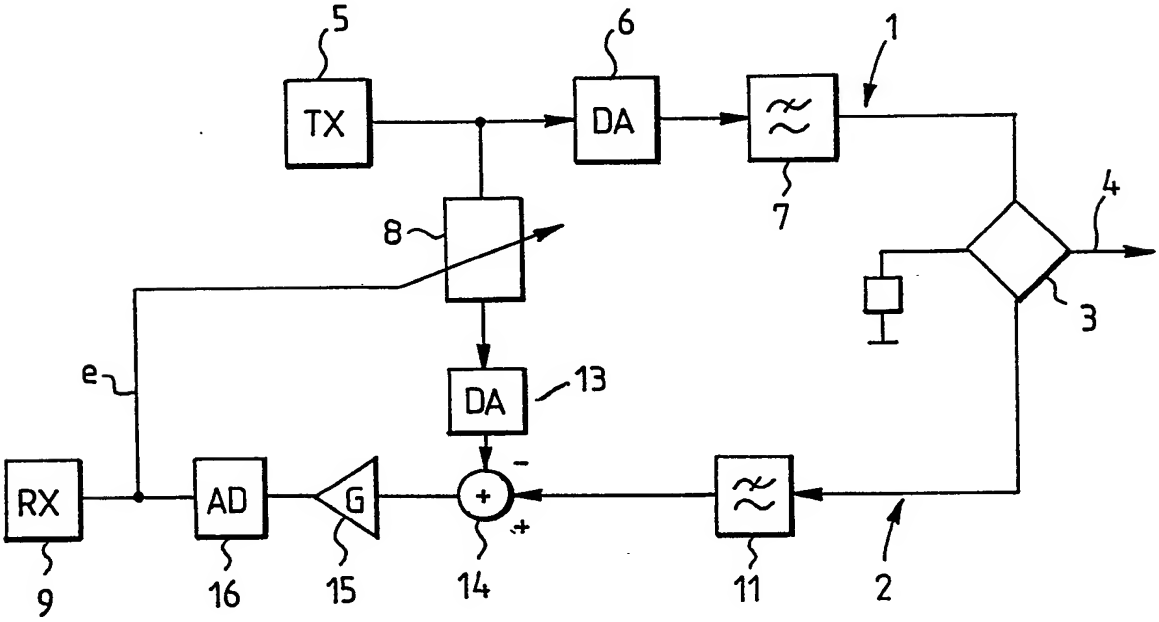
5
6
1
TX
DA
7
4
8
3
e
DA
13
RX
AD
G
9
16
15
14
11
2

FIG. 2

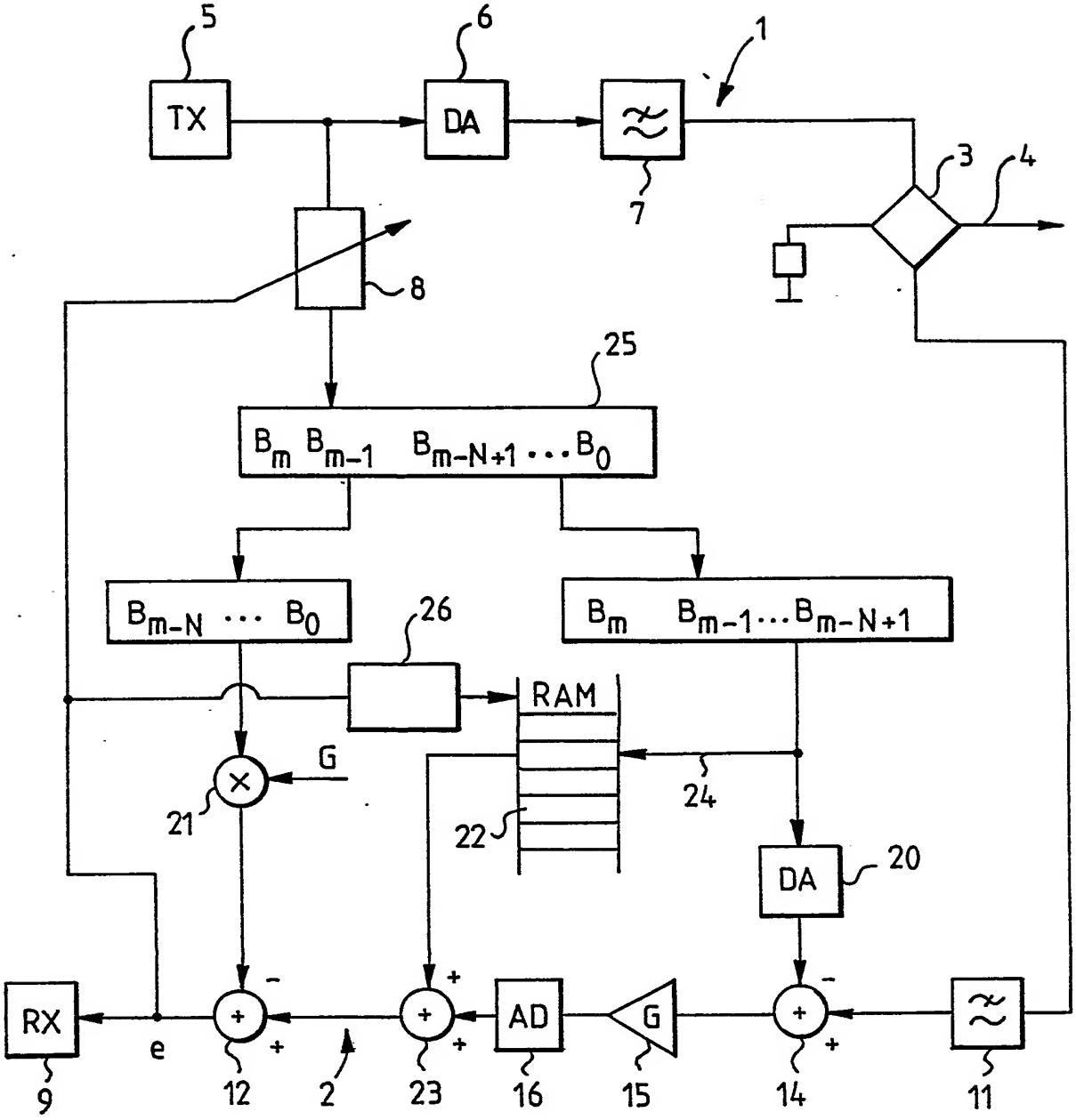
5
6
1
TX
DA
7
3
4
8
25
B_m B_{m-1} B_{m-N+1} ... B_0
B_{m-N} ... B_0
26
B_m B_{m-1} ... B_{m-N+1}
RAM
G
21
22
24
20
DA
RX
e
9
12
2
23
16
AD
15
G
14
11

FIG. 3

A method and device for echo cancellation in a transmission device, such as a modem

The present invention relates to a method and a device for echo cancellation in a transmission device, such as a modem. In the method, an echo estimate is formed of the transmitted signal and said echo estimate is subtracted from the received signal. The device of the method again comprises means for forming an echo estimate of the transmitted signal and means for subtracting said echo estimate from the received signal.

A typical operating environment where the method and device of the invention are used is a subscriber loop of a telephone network utilizing full-duplex transmission, but the invention may naturally be utilized in connection with other two-wire lines as well, for instance in local area networks. In such an environment, the receiving and transmitting branches of the transmission device have been connected via a line hybrid to a two-wire connection. When a transmitter at the transmitting branch transmits a signal via the line hybrid to the two-wire connection, the echo component of this signal is added to the signal received over the two-wire connection via the line hybrid, in which event the signal received over the line hybrid to the receiving branch comprises both the received effective signal (the signal coming from the transmitter of the opposite end) and the echo component of the transmitted signal.

The cancellation of the echo component from the received signal can in principle be effected in two different ways. In both ways, an estimate of the echo component in digital form is first formed in a separ-

ate echo canceller in response to a transmitted signal. The first way is to digitally subtract the echo estimate from the received signal, which has first been converted to a digital form with an A/D converter. Another way is to convert the echo estimate calculated by the echo canceller first to an analog signal and subtract the signal from the signal arriving over the line hybrid with an analog summing amplifier. To facilitate the understanding of the present invention, both of the known ways are described in more detail hereinbelow in the special part of the specification.

The drawback of the known echo cancellation methods described above is that high resolution requirements must be set on the necessary A/D and D/A converters, which again complicates the practical circuit arrangement.

The object of the present invention is to improve the known echo cancellation methods and devices so that the requirements set on the necessary A/D and D/A converters can be reduced and thereby the practical circuit arrangement simplified. With the method of the invention, this is achieved so that N most significant bits are separated from the echo estimate and the portion of the echo estimate corresponding to these is analogically subtracted from the received signal, and that the portion of the echo estimate corresponding to the remaining least significant bits is digitally eliminated from the received signal. The device of the invention is again characterized by that which is disclosed in the characterizing portion of the appended claim 4.

The main idea according to the invention is to divide the echo estimate into two parts and cancel analogically the majority of the echo. Thereby one

achieves a smaller number of D/A converter levels before the analog subtraction point, and as the dynamic range of the echo decreases after the subtraction point, also the requirements on the resolution of the A/D converter after the subtraction point are lower.

The reduction of the requirements on the resolution of the necessary A/D and D/A converters affords advantage particularly at high bit rates, with which the price of the converter will rapidly increase with the increase of the bit number, and in VLSI implementations wherein the silicon area increases as the resolution increases.

In accordance with a preferred embodiment of the invention, the accuracy requirement for the levels of the D/A converter can be further reduced so that the signal obtained as a result of analog subtraction is corrected by means of correction terms which can be read from memory.

In accordance with another preferred embodiment of the invention, the correction terms are adjusted continually. Thereby adaptation can be made to level changes in D/A converters resulting for instance from a temperature change.

The following is a more detailed description of the invention, with reference to examples according to the accompanying drawings wherein

Figure 1 illustrates a modem coupled to a two-wire connection, being provided with a known echo cancellation circuit wherein the echo estimate is digitally cancelled from a received signal,

Figure 2 illustrates a modem coupled to a two-wire connection, being provided with a known echo cancellation circuit wherein the echo estimate is analogically cancelled from a received signal, and

Figure 3 illustrates a modem coupled to a two-

wire connection, being provided with an echo cancellation circuit according to the invention.

Figure 1 shows a modem provided with a digitally accomplished echo cancellation circuit known per se, said modem comprising transmitting and receiving branches 1 and 2 respectively and being coupled to a two-wire connection 4 via a line hybrid 3, which two-wire connection may be for instance a subscriber line of a telephone network. In the transmitting branch 1, the transmitter 5 of the modem has been connected to the line hybrid via a D/A converter 6 and a low-pass filter 7. The output signal of the transmitter has been connected to an echo canceller 8 which forms an echo estimate in response to the transmitted signal. In the receiving branch of the modem, the signal coming over the hybrid 3 is connected to a receiver via a low-pass filter 11 and an A/D converter 10. There is a digital summing unit 12 between the receiver 9 and the A/D converter 10, in which summing unit the numerical echo estimate calculated by the echo canceller is subtracted from the output signal of the A/D converter 10. Since the echo level can be considerably higher than the level of the effective signal, an accurate A/D conversion is necessary in this solution in order for the accuracy of the effective signal to be sufficient. In practice, the necessary bit resolution of the A/D converter 10 is 12 to 16, depending on the application.

Figure 2 shows a modem provided with the other above-indicated echo cancellation circuit known per se. The same reference numerals have been used for the same parts as in connection with Figure 1. In this arrangement, the numerical echo estimate calculated by the echo canceller 8 is first converted to an analog signal with a D/A converter 13, and this

analog signal is subtracted from the signal coming through the line hybrid 3 with an analog summing amplifier 14. The bit resolution required of the D/A converter 13 is 12 to 16, depending on the application. After the summing amplifier 14 there is an analog amplifier 15 in the receiving branch, wherewith the level of the signal having a reduced dynamic range after the subtraction is increased. The signal thus obtained is applied to an A/D converter 16, wherewith it is converted to a digital form. The output signal over the A/D converter is transmitted to a receiver 9 and to the control circuit of the echo canceller 8. The bit resolution required of the A/D converter 16 is lower than in the case of Figure 1, i.e. about 6 to 10, depending on the application.

In the case of both Figure 1 and Figure 2, the signal to be received includes after the subtraction point of the echo estimate the effective signal sent by the opposite end as well as an echo residual error resulting from the incomplete setting of the echo canceller. As the effective signal and the residual error of the echo are uncorrelated, the residual error can be "dug out" by correlating the residual error and the transmitted signal with one another. For this purpose, the residual error which has been denoted in Figures 1 and 2 with the reference character e is fed to the echo canceller 8 whose regulation will seek to minimize said residual error.

The known echo cancellation methods described above have also been described in U.S. Patent 4 669 116, which relates to the formation of an echo estimate.

In Figure 3, a modem has been provided with an echo cancellation circuit according to the invention. The same reference numerals have been used for the

corresponding parts as above. A numerical echo estimate (of a length of m+1 bits) is received from the echo canceller 8 in a manner known per se, said echo estimate being denoted by the reference $B_mB_{m-1}...B_{m-N+1}...B_0$ wherein B_m is the most significant bit and B_0 the least significant bit, respectively. In the branching block 25, N most significant bits $B_mB_{m-1}...B_{m-N+1}$ are separated from the echo estimate, and these are inputted in an N-bit D/A converter 20. The signal generated by the converter 20 is subtracted in analog from the incoming signal received through the hybrid 3 in the summing amplifier 14. After the subtraction, the received signal is amplified with an analog amplifier 15 having an amplification factor G and converted with an A/D converter 16 to a numerical form. When the echo cancelling D/A converter 20 has N bits, the dynamic range of the echo decreases after the analog echo cancelling point 14 about 20 $\log_{10}(2^N)$ dB, whereby the bit resolution required of the A/D converter 16 is reduced.

The lowest bits $B_{m-N}...B_0$ of the echo estimate, which were omitted from the control of the D/A converter 20, are multiplied numerically with the amplification factor G in a multiplier 21, and the portion of the echo estimate thus produced is subtracted from the received signal in a digital summing unit 12.

By dividing the echo estimate into two parts, the number of levels (2^N) in the D/A converter 20 can be diminished. However, to achieve accurate echo cancellation the levels of the D/A converter must still be accurate. Yet it is easier to achieve a D/A converter having accurate levels but a shorter control word than a converter having a long control word.

In accordance with a preferred embodiment of the invention, the practical circuit realization can

be further simplified by compensating the inaccuracies of the D/A converter by means of correction values to be read from memory. By this means, the requirements set on the levels of the D/A converter can be reduced. For this purpose, the device according to the invention holds 2^N correction values in the RAM memory 22. Of the N bits fed to the D/A converter 20, the address of said RAM table is formed in the control line 24, in which case the correction term corresponding to the employed level generated by the D/A converter 20 can be looked up from the table, which term is then numerically added to the received signal in a digital summing unit 23.

In principle, values calculated in advance could be used as correction terms, but it is however more advantageous to adjust the correction terms maintained in the RAM memory 22 continually, since in this way the echo cancellation is able to adjust itself to the change in the levels of the D/A converter caused by a temperature change and also to changes in the amplification coefficient of the analog amplifier 15. To illustrate the adjustment, the error signal at moment i is indicated with the reference character e_i and the control word for the D/A converter 20 with the reference character X_i, and thus the correction term $RAM(X_i)$ is used. The adjustment of the correction term takes place in accordance with the invention as follows:

$$RAM(X_i) \rightarrow RAM(X_i) - \Delta e_i,$$

wherein Δ is the scaling factor. A new correction term is thus obtained when the value of the error signal multiplied by the scaling factor is subtracted from the correction term employed at each moment. The block performing the regulation whereinto the error signal e_i is fed has been denoted by reference numeral

26 in Figure 3. The adjustment may also be realized by software.

The error signal e_i also contains the effective signal arriving from the opposite end of the two-wire line. This effective signal is uncorrelated with the control word X_i and the value of the required correction term $RAM(X_i)$, as a result of which it will be averaged out when the correction terms are adjusted continually. The selected scaling factor Δ of the error must be sufficiently small, so that the (zero average) fluctuation of the correction term caused by the effective signal is of so low a level that it will not interfere with the operation of the echo cancellation circuit. It can be shown that the variance of the correction term = $(\Delta\ \sigma_r^2)/2$, wherein Δ is the above-stated control step and σ_r^2 is the efficiency of the effective signal. From this expression, one can calculate the size of the control step for the desired effective/interference signal ratio. For instance, when one wishes the interference to be 30 dB below the effective signal, the size of the control step will be Δ=0.002.

Even though the invention has been explained in the foregoing with reference to an example according to the accompanying drawing, it is evident that the invention is not restricted to said example but can be modified in many ways within the scope of the inventive idea disclosed in the appended claims. For instance, the branching block 25 can be realized, except by means of digital logic, also by software. Also the echo estimate can be formed in many different ways. A typical way of realizing the echo canceller is an adaptive FIR filter. Other known means have been disclosed in U.S. Patent 4,669,116 referenced at the beginning of this specification. Also, the

transmission device need not necessarily be a modem, but other means (which may have a built-in modem) are possible as well.

Claims:

1. A method for echo cancellation in a transmission device, such as a modem, wherein an echo estimate ($B_mB_{m-1}...B_{m-N+1}...B_0$) is formed of the transmitted signal and said echo estimate is subtracted from the received signal, c h a r a c t e r i z e d in that N most significant bits ($B_mB_{m-1}...B_{m-N+1}$) are separated from the echo estimate and that part of the echo estimate which corresponds to these is analogically subtracted from the received signal, and that the portion of the echo estimate corresponding to the remaining least significant bits ($B_{m-N}...B_0$) is digitally eliminated from the received signal.

2. A method as claimed in claim 1, c h a r a c t e r i z e d in that the signal obtained as a result of analog subtraction is corrected by means of correction terms (RAM(X_i)) read from memory.

3. A method as claimed in claim 2, c h a r a c t e r i z e d in that the correction terms are adjusted continually.

4. A device for echo cancellation in a transmission device, such as a modem, comprising means for forming an echo estimate ($B_mB_{m-1}...B_{m-N+1}...B_0$) from a transmitted signal, and means for subtracting said echo estimate from the received signal, c h a r a c t e r i z e d in that it comprises in combination:

- means for analogically subtracting the portion of the echo estimate ($B_mB_{m-1}...B_{m-N+1}...B_0$) corresponding to the most significant bits ($B_mB_{m-1}...B_{m-N+1}$) thereof from the received signal, and
- means for digitally subtracting the portion of the echo estimate corresponding to the

least significant bits ($B_{m-N}...B_0$) thereof from the received signal.

5. A device as claimed in claim in claim 4, c h a r a c t e r i z e d in that it comprises a memory (22) wherein correction terms ($RAM(X_i)$) are stored, and a digital summing unit for adding/ subtracting said correction terms from the received signal.

6. A device as claimed in claim 5, c h a r - a c t e r i z e d in that it includes means for continual adjustment of the correction terms.

7. A method for echo cancellation in a transmission device substantially as hereinbefore described with reference to Figure 3 of the accompanying drawings.

8. A device for echo cancellation in a transmission device substantially as hereinbefore described with reference to Figure 3 of the accompanying drawings.

Patents Act 1977
Examiner's report to the Comptroller under Section 17 (The Search Report) - 12 -

Application number

9125366.6

Relevant Technical fields

(i) UK Cl (Edition K) H4R:RLES

(ii) Int CL (Edition 5) H04B

Search Examiner

ALAN STRAYTON

Databases (see over)

(i) UK Patent Office

(ii)

Date of Search

3 JUNE 1992

Documents considered relevant following a search in respect of claims ALL

Category (see over)	Identity of document and relevant passages	Relevant to claim(s)
	NONE	

Category	Identity of document and relevant passages	Relevant to claim(s)

Categories of documents

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